# Inverse Metal-Assisted Chemical Etching Produces Smooth High Aspect Ratio InP Nanostructures

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**S** Supporting Information

**ABSTRACT:** Creating high aspect ratio (AR) nanostructures by top-down fabrication without surface damage remains challenging for III–V semiconductors. Here, we demonstrate uniform, array-based InP nanostructures with lateral dimensions as small as sub-20 nm and AR > 35 using inverse metal-assisted chemical etching (I-MacEtch) in hydrogen peroxide ($H_2O_2$) and sulfuric acid ($H_2SO_4$), a purely solution-based yet anisotropic etching method. The mechanism of I-MacEtch, in contrast to regular MacEtch, is explored through surface characterization. Unique to I-MacEtch, the sidewall etching profile is remarkably smooth, independent of metal pattern edge roughness. The capability of this simple method to create various InP nanostructures, including high AR fins, can potentially enable the aggressive scaling of InP based transistors and optoelectronic devices with better performance and at lower cost than conventional etching methods.



**KEYWORDS:** InP, metal-assisted chemical etching, MacEtch, inverse MacEtch, I-MacEtch, MACE, nanowires, finFET
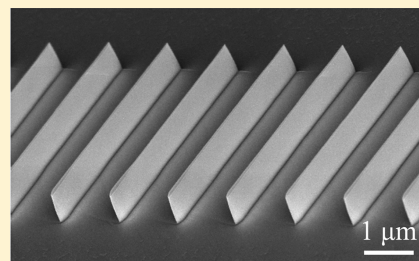
Since 2000, semiconductor micro- and nano-fabrication schemes based on the metal-assisted chemical etching (MacEtch) approach for localized material dissolution have been the focus of extensive research.[1−3] The MacEtch mechanism, fundamentally, relies on noble metal (typically Au, Pt, or Ag) catalysis of an oxidation reaction in a semiconductor.[1,2] Upon oxidation of the semiconductor, preferential material removal can then take place through solution-based etching. Because the noble metal of choice can be patterned directly on semiconductor surfaces by way of conventional nanofabrication procedures, such as electron-beam lithography (EBL)[4,5] or soft-lithography (SL),[6,7] site-specific etching can, therefore, be realized in a single solution containing an oxidant and an etchant (typically an acid).[6,8] Thus, submerging the metal-coated semiconductor within a MacEtch solution will cause the patterned metal to sink into the substrate, thereby leaving behind semiconductor nanostructures that are complementary to the metal pattern.

The MacEtch mechanism has been established as an attractive alternative to standard plasma-assisted etching approaches. MacEtch provides a low-cost, room-temperature, and vacuum-condition-free substitute to reactive-ion etching (RIE) that is also devoid of the risk of generating undesired ion-beam induced damage,[9,10] irregular sidewall features, and nonvertical etch profiles.[11,12] Because material etching is an essential requirement for semiconductor device fabrication, MacEtch has the potential to impact a number of highly relevant technological fields such as photonics,[13,14] optoelectronics,[15] microfluidics,[16] and photovoltaics.[17−19] In fact, in recent years, numerous device applications relying on MacEtch

processing have been demonstrated, including solar cells,[19] light-emitting diodes (LEDs),[7] biosensors,[20] photonic crystal reflectors,[8] and Li-ion batteries.[21]

Research in this field has, thus far, been predominantly concentrated on the MacEtch of Si[22−27] and $Si_xGe_{1−x}$ alloys.[28] However, more recently, metal-catalyzed wet etching of III–V compound semiconductors such as GaAs[6,7] and GaN[29,30] have also been demonstrated. This not only validates the capability of the technique for processing of pertinent optoelectronic materials but also allows for a deeper understanding of the underlying MacEtch chemistry to be uncovered. As such, one of the main challenges in MacEtch research remains the extension of this etching technique to applications involving other III–V semiconductors, such as InP.

In addition to being the primary functional material of the telecommunications lasers industry, InP has also been established as a key material for next-generation high-frequency nanoelectronics[31,32] and photovoltaics[33,34] due to its high carrier mobility and low surface recombination velocities in comparison to other III–V materials with comparable bandgap energies. Yet, development of InP nanostructures has required either bottom-up crystal growth processes,[33,34] or top-down RIE-based methods,[35,36] both of which are associated with the handling of toxic gases, high-vacuum conditions, and high-temperature reactions. Anodic etching of InP to generate nanomembranes was also demonstrated very recently.[37] To

date, MacEtch of InP has hardly been studied, except for one report by Asoh et al. where periodic InP microbump (~30 $\mu$m in width, ~10 $\mu$m in height, and 63 $\mu$m in center-to-center spacing) arrays were formed through UV irradiation-assisted Pt-MacEtch.[38] This work, in which the role of metal type (Au, Pd, and Pt) on etching rate was also explored, has opened the possibility of etching InP by MacEtch. However, the sidewalls of these microbumps lack smoothness and verticality. Moreover, scaling to the nanometer scale while generating high aspect ratio (AR) features will be required for high-performance electronic device applications.

Here, we present the fabrication of a wide variety of InP nanostructures with smooth sidewalls, lateral dimensions as low as sub-20 nm, and AR greater than 35:1, by a systematic I-MacEtch method without UV irradiation. The term I-MacEtch is coined to describe the etching mechanism whereby a patterned metal layer acts as a catalyst as well as a mask for the formation of features in an inverse arrangement to that expected of traditional MacEtch. Thus, the I-MacEtch mechanism causes the semiconductor regions not interfaced with the catalyst layer (i.e., between the metal covered areas) to be preferentially etched. In addition, the areas directly underneath the metal catalyst/mask can be etched (laterally) simultaneously at a fixed ratio relative to the vertical etch rate determined by the I-MacEtch conditions. This feature can result in high AR nanostructures that are much narrower than the metal pattern with sidewall smoothness not at all limited by the metal pattern edge roughness. We report on the effects of two types of metal catalysts, etching solution chemistry, etching period, areal coverage and separation of the metal patterns, and metal pattern orientation as related to the crystallographic orientation of the substrate, on the etch rate and morphology of the resultant InP nanostructures. The inverse nature of the MacEtch phenomenon observed here is attributed to the presence of a thick and insoluble oxide layer formed at the metal/semiconductor interface, which effectively serves as a barrier to limit hole injection in the vertical direction. Furthermore, a qualitative model is presented for the etching mechanism and routes toward device applications utilizing the I-MacEtch approach are outlined.

Sulfur-doped (n-type) InP (100) substrates with doping levels between $0.8-8.0 \times 10^{18}$ cm$^{-3}$ were used for all etching experiments. Prior to metal patterning, all InP wafers were first immersed into a diluted HF solution for native oxide removal and subsequently degreased with standard solvents. The substrates were then patterned via soft lithography (SL), through a previously established process.[6] After a thin layer of photocurable epoxy (SU-8) was spin-coated on the InP substrates, a polydimethylsiloxane (PDMS) stamp was pressed against them. The substrates were then soft-baked at 95 °C. The depressed photoresist (8% SU-8) in the patterned window regions was removed by oxygen plasma RIE, followed by electron-beam evaporation of a 30 nm thick metal (Pt or Au, as specified below) film. An acetone liftoff process then resulted in arrays of square metal pads with widths of ~1.1 $\mu$m and having separations of ~300 nm. The size of each array was $1.5 \times 1.5$ cm$^2$ and the following experiments were performed with the same patterns as defined above, unless otherwise specified. It is noted that electron-beam lithography (EBL) was used for the experiments with non-square patterns such as lines and rings, as shown in the following sections. The EBL samples were prepared with PMMA resist followed by electron-beam exposure and oxygen plasma etching to fully open the exposed

windows. The metal layers were then deposited in an identical evaporation process as that used for SL-prepared samples. After patterning, I-MacEtch was performed in a mixed solution of hydrogen peroxide (H$_2$O$_2$) as an oxidizing agent and sulfuric acid (H$_2$SO$_4$) as a dissolution agent. All I-MacEtch experiments were performed at room temperature. For the sake of convenience in the following discussions, we define $\gamma = [\text{H}_2\text{SO}_4]/[\text{H}_2\text{O}_2]$, where [H$_2$SO$_4$] and [H$_2$O$_2$] are the molar concentrations of each solution with units of mol/dm$^3$. The arrays of InP nanopillars were then imaged by scanning electron microscopy (SEM; Hitachi S-4800). The optical and structural qualities of such nanostructures were characterized through micro-photoluminescence ($\mu$-PL) and high-resolution transmission electron microscopy (HR-TEM), respectively. HR-TEM characterization was carried out using a JEOL 2010-F microscope, using TEM samples prepared by ultrasonication of InP nanopillars in a small volume of methanol and subsequent deposition on lacey-carbon TEM grids. All $\mu$-PL measurements were performed at room temperature using a Renishaw inVia PL system, equipped with a CCD camera with excitation provided by a 633 nm HeNe pump laser.

A set of SEM images in Figure 1 show several types of nanostructures obtained by etching n-InP wafers containing
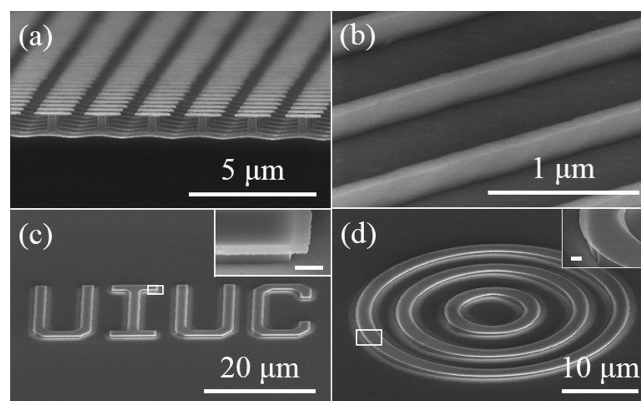


**Figure 1.** InP nanostructures generated from I-MacEtch: (a) arrays of nanopillars generated from Pt square pads, (b) arrays of nanoscale fins from Au lines after Au removal, (c) the letters "UIUC" from Au pads with inset showing a high-magnification view of the outlined region (white box) corresponding to the letter "I", and (d) concentric InP microstructures generated from a set of Au rings, with inset showing the high-magnification view of the outlined region. The inset scale bars are 500 nm and metal catalyst layers were patterned by SL (a) and EBL (b−d).

either SL- or EBL-prepared metal patterns in a solution of H$_2$SO$_4$ and H$_2$O$_2$. The structures include highly ordered arrays of nanopillars from ~1.1 $\mu$m$^2$ Pt square pads (Figure 1a; note that the InP pillars are directly beneath the Pt pads), arrays of nanoscale fins after Au removal (Figure 1b), microscale mesas forming the letters UIUC (Figure 1c; inset shows a high-magnification view of squared area from the letter 'I' where the InP block sits directly beneath the Au pad), and circular InP microstructures from concentric Au rings (Figure 1d). These images demonstrate that the I-MacEtch process can be implemented to fabricate three-dimensional (3D) InP micro- and nanostructures from various metal patterns, whether the pattern is linear, circular, discrete, or continuous.

The conventional MacEtch mechanism has been widely reported to be the product of two steps: a charge transfer

process and a mass transfer process.[2] The charge transfer process includes hole generation and injection, the rate of which is affected by the type of metal catalyst, semiconductor, and oxidant. On the other hand, mass transfer is a process determined by the diffusion of dissolution reagents and reaction byproducts, primarily influenced by solution components, semiconductor structure, and geometrical access. Both transfer processes must be optimized for the generation of controlled etching profiles. In order to better define the nature of the I-MacEtch mechanism and to optimize the etching process, we explore the effects of (1) metal type, (2) metal pattern orientation relative to the crystallographic orientation of the semiconductor, (3) etching solution concentrations, and (4) etching period. The specific influence of each of these variables is explored in the following sections.

The comparison of two noble metals widely used for MacEtch, Pt and Au, is studied first. The Pt and Au layers were patterned by SL on the InP substrates in Figure 2a and 2b, respectively. The samples were then etched under identical conditions; namely, in MacEtch solutions of $\gamma = 24.5$ for 30 min at room temperature. As clearly seen in Figure 2, etching took place in both vertical and lateral directions with different etch rates for different metals. The nanopillars formed using Pt as



**Figure 2.** Cross-sectional SEM images of InP pillar arrays formed by I-MacEtch with metal catalyst patterns (sitting on top) made of (a) 30 nm thick Pt and (b) 30 nm thick Au disks. (c) I-MacEtch control experiment: SEM shows no etching with SU-8 as a mask. Inset scale bars represent 1 $\mu$m.

the catalyst are ~0.61 $\mu$m in height and ~0.33 $\mu$m in width with near-vertical sidewalls. In contrast, those formed using Au as the catalyst are only ~0.29 $\mu$m tall and the tapered sidewall profiles are revealed with bottom widths of ~1 $\mu$m and top widths of ~0.87 $\mu$m. Tapered anisotropic wet-etching behavior of InP had been reported previously using HCl-based solutions through the use of a lattice-matched InGaAs layer as an etching mask and was attributed to a crystal orientation-dependent etch rate.[39] The etch profile observed here in the presence of metals can be explained by the competition between oxidation and material dissolution during etching. It is well known that the etch rates are enhanced if a metal with a higher work function is used as a catalyst during MacEtch of Si,[1] GaN,[40] and InP.[38] In this study, both vertical and lateral etch rates of InP using Pt are faster than those when Au is used, as expected from experimental work functions of 5.65 and 5.1 eV for Pt and Au, respectively.[41] The use of Pt rather than Au results in a greater rate of hole injection and, therefore, a faster etch rate. Consequently, crystallographic etch rate dependences are effectively mitigated, such that vertical sidewalls can be exposed (Figure 2a). In contrast, the use of Au as a catalyst reduces the hole generation rate and causes the process to be oxidation-limited. This results in the formation of sidewall profiles that exhibit preferential crystallographic etch rate dependences, as shown in Figure 2b. Note that when identical mask patterns made of SU-8 were used under the same etching conditions, no visible etching could be observed, as shown in Figure 2c. This confirms the catalytic role of the metal mask in I-MacEtch.

To employ these nanostructures for device applications, the metal layer typically has to be removed during subsequent device fabrication process flows.[7,8] As explained further in the Supporting Information (Section 1), well-known Pt etchants, such as aqua regia and piranha solutions,[42] are incompatible with InP. On the other hand, Au catalyst layers can be removed using standard Au etchants (Transene Co.) without attacking InP. Therefore, in order to establish etching protocols that are conducive to future device fabrication processes, the following I-MacEtch experiments are conducted with Au only, unless otherwise stated.

The crystallographic dependence of etching profiles is detailed next as a function of mask pattern orientation. Arrays of Au squares were patterned to have two different orientations with the square edges aligned at 45 and 90° relative to the (110) wafer flat. In this orientation study, the etch time was 10 min and the samples were etched in a solution of $\gamma = 24.5$. Figure 3 shows SEM images (after Au removal) obtained at plan-view (a,d), low-magnification 45° tilted-view (b,e) and high-magnification 45° tilted-view (c,f) of InP nanostructures formed by I-MacEtch using the two distinct pattern orientations indicated. Note that the pattern orientations shown in Figure 2 are the same as Figure 3d. It can be seen that vertical sidewalls on all four sides are achieved (Figure 3c), where the Au patterns are oriented at 45° relative to the wafer flat, so that the low-index {010} planes are the facets most exposed to the etching solutions. Conversely, when the Au patterns are oriented at 90° relative to the primary (110) flat (Figure 3f), in addition to the perpendicular {010} planes, as in the case of purely masked, wet etching,[39] sloped facets that are presumably the slow etch (211)A facets are also produced. Thus, only the 45° orientation of the metal patterns is suitable for the formation of perfectly vertical nanostructures having (100) sidewall facets, while a 90° orientated metal patterns lead to the formation of features having multifaceted geometries
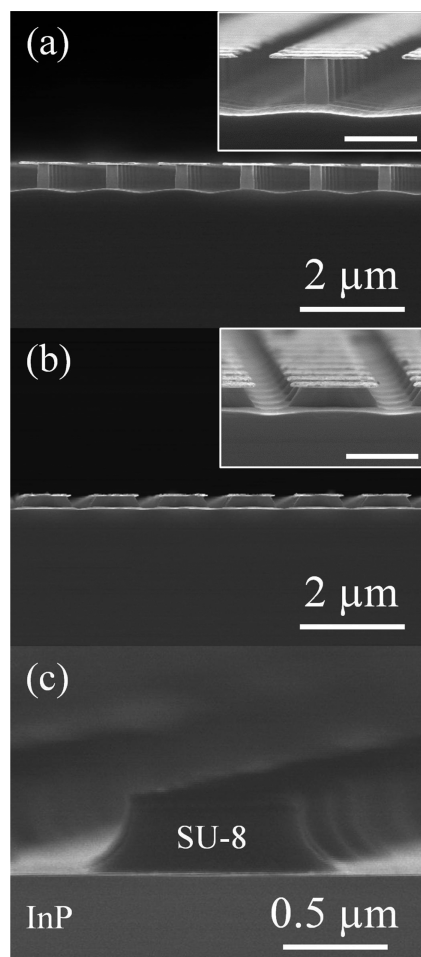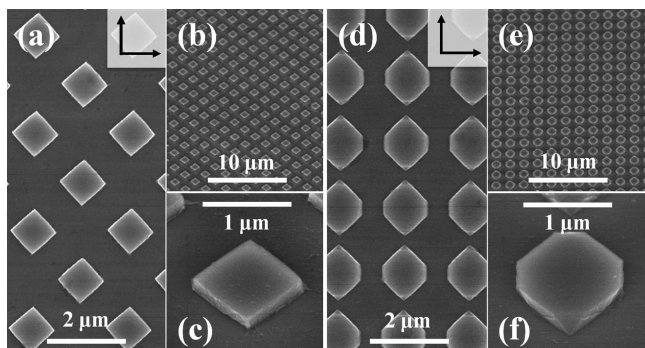
**Figure 3.** SEM images of InP nanostructures etched for 10 min with $\gamma$ = 24.5 at room temperature, where the square Au catalyst patterns (removed before SEM) were aligned at (a–c) 45° and (d–f) 90° relative to the (110) wafer flat (the two arrows in the top-view images indicate equivalent ⟨110⟩ directions). (a,d) panels show plan-view images, while (b,c,e,f) were obtained at a 45° tilted angle.

with high-index sidewall facets. Asoh et al. had also noted crystal orientation-dependent anisotropic etching in their study of Pt-assisted InP etching.[38] We emphasize that these types of structures can only be formed in I-MacEtch solutions wherein the oxidant concentration is sufficiently low and the etch rate is limited by hole generation. Such conditions are more conducive to a preferential, masked wet-etching process rather than a catalyst-assisted etching phenomenon. This is further explored in the subsequent study of the I-MacEtch solution chemistry.

To better study this effect, vertical and lateral etch rates were measured as a function of concentration ratio, $\gamma = [H_2SO_4]/[H_2O_2]$, as shown in Figure 4a,b for metal mask orientations of 45 and 90°, respectively. All data points in this paper represent averaged measurements from sets of 25 pillars with error bars showing one standard deviation unless otherwise specified. Wafer-to-wafer reproducibility was confirmed for numerous (>10) wafers etched in the same batch as well as from batch-to-batch. Lateral etch rates are defined based on the separation of the Au pattern edge from the furthest laterally etched InP plane and the etching duration. The values of $\gamma$ used are 5.7, 14, and 24.5 with a constant etching time of 20 min, and etching is performed at room temperature. We note that if the ratio, $\gamma$, is beyond 24.5, the oxidant concentration becomes negligibly

small, such that no discernible etched nanostructure formation occurs. On the other hand, when the value is below 5.7, no etching occurs due to insufficient acid concentrations and, thus, inadequate oxidized material dissolution. This is true regardless of pattern orientations.

For the 45° oriented metal patterns (Figure 4a), both the vertical etch rates (VER) and lateral etching rates (LER) increase with $\gamma$ almost linearly, indicating that mass transfer is the rate determine step. For the 90° oriented patterns (Figure 4b), under identical conditions the VER stays relatively constant at ~25 nm/min, while a dramatic decrease can be seen in the LER. The results from ref 38 were plotted in Figure 4b as filled symbols for comparison. In order to achieve nanostructures with high AR, the lateral etch should be suppressed with substantially higher VERs. Interestingly, the VERs are consistently higher than the LERs for 45° oriented patterns, while the VER/LER > 1 condition is only satisfied after a certain threshold of $\gamma \geq 19$ for 90° oriented patterns. We believe that this is related to the direct exposure of the slow-etch (211)A facets to the etching solution.[39] As a result, the dramatic decrease of LER (from ~60 to ~10 nm/min) is observed as $\gamma$ increases (i.e., reduction of oxidant concentration), as fewer holes are generated at a lower proportion of $[H_2O_2]$. Focusing on high-AR nanostructures with vertical sidewall profiles, the $\gamma$ = 24.5 solution and 45° oriented patterns are used for further experiments.

Figure 5 shows the evolution of InP nanopillar geometries in the I-MacEtch solution optimized above by plotting the average heights and widths measured as a function of etching duration. The etching depth increases almost linearly for the first 10 min of etching, beyond which the VER (Figure 5a) exhibits a distinct saturation trend. Similarly, as shown in Figure 5b, the LER also decreases and saturates in time. The influence of metal catalyst size and separation is presented in the Supporting Information. By increasing the Au catalyst square pad size from 1 to 5 $\mu m$, a monotonic increase in etching depth was observed. On the other hand, the separation of Au catalyst pads did not affect the etching rate in the range studied (0.75–3 $\mu m$).

The sidewall structure of the I-MacEtched nanofeatures was evaluated via TEM. Figure 6 shows TEM images obtained from the sidewall facet (Figure 6a) and top facet (Figure 6b) of an I-MacEtch-fabricated single InP nanopillar. All TEM experiments
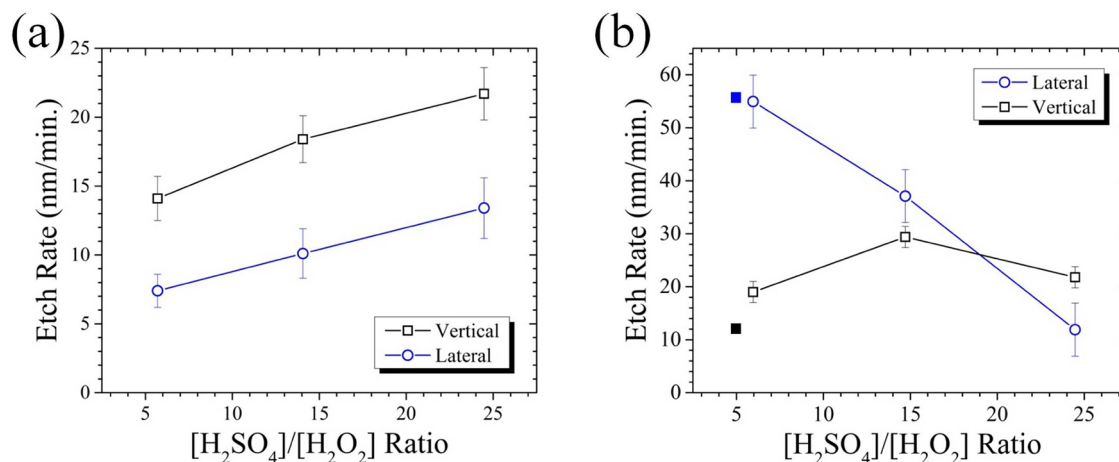


**Figure 4.** Plots of vertical and lateral etch rates as a function of $\gamma = [H_2SO_4]/[H_2O_2]$, when the Au squares are patterned to be oriented at (a) 45° and (b) 90° relative to the (110) flat on (100) InP substrates. The data represented by the filled square points in (b) are taken from a previous report[38] on MacEtch of InP (with UV irradiation) for comparison.
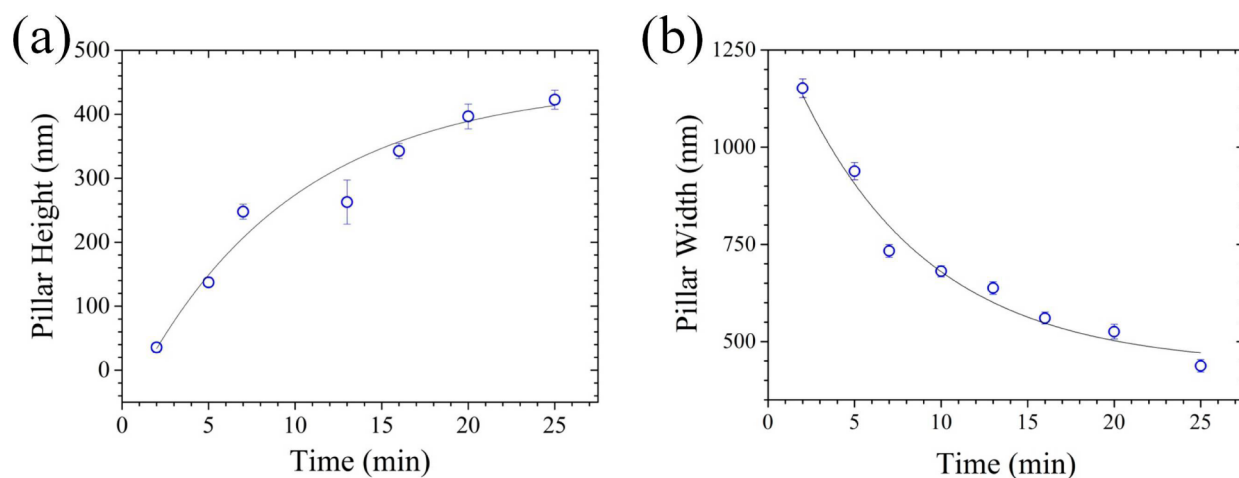
**Figure 5.** Plots of average (a) height and (b) width of InP nanopillars as a function of I-MacEtch time in the optimized ($\gamma = 24.5$) solution with fitted trend lines.
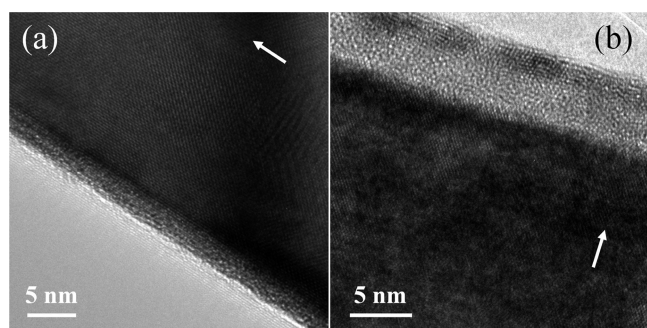


**Figure 6.** HR-TEM images obtained from the (a) sidewall and (b) top surface of an I-MacEtched single InP nanopillar after Au removal. The white arrows point toward the top of the nanopillar.

were performed after removing the Au catalyst layer by wet-etching. In both panels of Figure 6, the white arrow points toward the top of the nanopillar. We emphasize that the nanopillar sidewalls exhibit an atomically smooth facet with no signs of surface damage or porosity. In addition, PL emission has been observed at room temperature from single ultrathin nanopillars (Supporting Information, Figure S3), confirming the optical quality of the I-MacEtched surfaces.

Notably, as shown in Figure 6b, after I-MacEtch and catalyst layer etching, an approximately 5.4 nm thick amorphous layer, presumably oxide, is observed at the top of the nanopillar. This layer is ~4 nm thicker than the native oxide layer formed on an (100) InP surface.[43] We attribute the formation of such a thick oxide layer to the oxidation of InP at the interface with the metal catalyst during I-MacEtch. Importantly, this oxide layer was not dissolved in the presence of $H_2SO_4$ (i.e., the acid in the I-MacEtch solution).

The existence of this thick oxide layer at the surface directly below the metal catalyst prevents any further oxidation (i.e., stops regular MacEtch from proceeding in the forward manner). As a result, the generated holes at the metal catalyst surface can only diffuse to areas between the metal-covered regions. The inverse nature of the InP MacEtch mechanism, therefore, has to be rooted in the formation of this thick
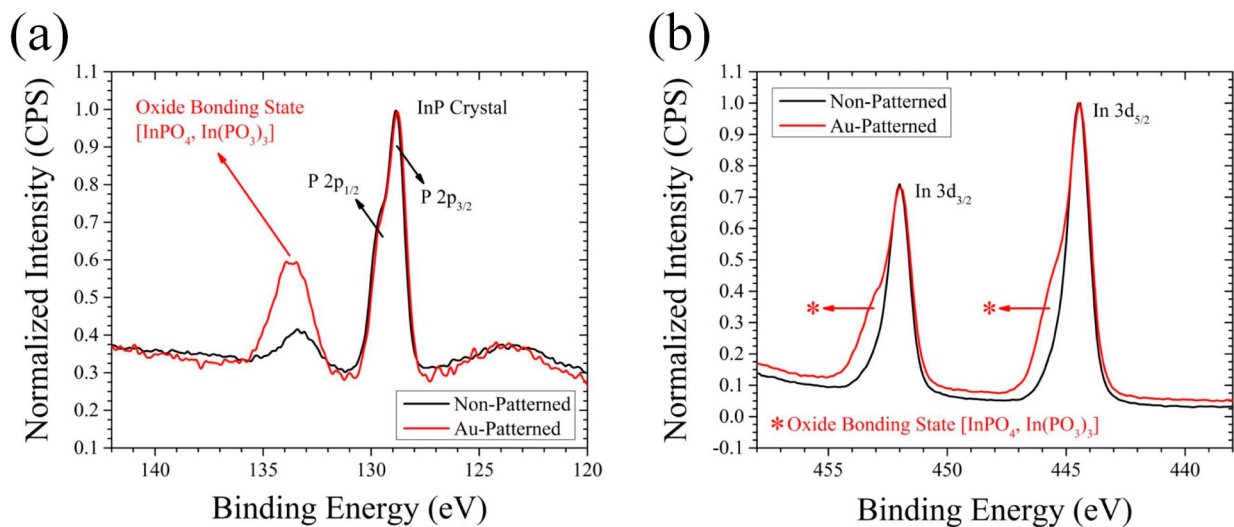


**Figure 7.** High-resolution X-ray photoelectron spectra showing the (a) P 2p and (b) In 3d bonding states. The red (black) curve corresponds to regions that had been Au-patterned (Au-free) during the I-MacEtch process. In both spectral regions, P-based oxide bonding states are prevalently detected in sample areas that were directly underneath the catalyst layer.

insoluble oxide layer at the metal−InP interface. As a comparison, silicon dioxide readily dissolves in Si MacEtch solutions containing HF,[2] and oxidized GaAs is soluble in GaAs MacEtch solutions, which also contain HF.[6]

It is known that different oxidation approaches produce different kinds of oxides for InP. For example, anodic oxides mainly consist of $In_2O_3$ and $P_2O_5$, while mixture combination of $In_2O_3$ and $InPO_4$ are formed in thermal oxides.[44] In order to further determine whether or not the thicker oxide layer formed at the Au/InP interface during I-MacEtch differs in composition from the thin native oxide present elsewhere, X-ray photoelectron spectroscopy (XPS) experiments were carried out. Figure 7a,b shows normalized high-resolution photoelectron core-level spectra in the regions of the P 2p and In 3d bonding states, respectively, obtained from InP surfaces that were Au-patterned (thicker oxide, red curves) and nonpatterned (exposed InP surface with native oxide, black curves) during I-MacEtch. In Figure 7a, the P 2p level signature, indicative of In−P bonding in the bulk crystal,[45] is clearly seen at 131 eV from both surface regions, while an additional oxidation state is found at 134 eV, which is detected with roughly 3-fold intensity in the Au-patterned region, in comparison to the Au-free region. The peaks at 134 eV correspond to P−O bonding states present in $InPO_4$, $In(PO_3)_3$, and $In(PO_3)_4$ compounds.[45−47] Similarly, in Figure 7b, in addition to the prominent bulk-crystal-like In $3d_{3/2}$ and In $3d_{5/2}$ levels at 452 and 444 eV, respectively, high-energy shoulder peaks at ∼446 and ∼453 eV are observed in the Au-patterned surface region, which are also signatures of $InPO_4$, $In(PO_3)_3$, and $In(PO_3)_4$ compounds.[45−47] Further analysis and curve fitting of high-resolution photoelectron spectra, as well as wider-range survey spectra are shown in the Supporting Information (Figure S5). The XPS results indicate that an excess of P-based oxides are formed upon I-MacEtch where InP is interfaced with Au, as opposed to the presence of mainly In-based oxides ($In_2O_3$) elsewhere. Likewise, Shibata and Ikoma have reported that the Xe arc lamp illumination enhances the formation of P-based oxides.[48] Similar to the case of illumination-mediated InP oxidation, we believe that Au catalysis forces the formation of an interfacial, P-based oxide layer that cannot be dissolved in $H_2SO_4$ during I-MacEtch, which also acts as a mask for InP etching in the I-MacEtch solution employed here. In fact, such a "masking" oxide layer has been directly observed via SEM imaging of InP fin-structures after the post-I-MacEtch Au-removal step (Supporting Information, Figure S6a). The residual, P-based oxide layer can be dissolved in HF following Au etching, as a final cleaning step to reveal the atomically smooth sidewalls of I-MacEtch-generated InP nanostructures (Supporting Information, Figure S6b).

In addition to the chemical nature of the InP I-MacEtch process discussed above, the energy band diagram of the Au−InP interface is analyzed in the Supporting Information (Section 8). In terms of hole injection barriers, our analysis indicates that InP has a much higher injection barrier for holes to overcome across the metal/semiconductor interfaces, as compared to Si. In other words, InP has a lower hole injection rate than Si. This slow oxidation rate may be responsible for the P-rich oxide formation at the Au/InP interface, which is not dissolved in $H_2SO_4$ and, thus, responsible for the prevalent inverse etching behavior.

Clearly, the etching behavior reported here is drastically different from conventional MacEtch, where the plane of hole injection progresses with the etch-front. In the case of I-MacEtch, the plane of hole generation (i.e., the Au surface) remains static and does not sink during etching. This results in a finite depth that the catalytic oxidation reaction can reach, thereby setting a vertical etch limit, while lateral etching continues independently, enabling high AR structures with ultrafine lateral dimensions. In contrast to conventional wet etching using a non-catalytic metal as the mask, first, etching does not occur in the I-MacEtch solution used here without the presence of a metal catalyst for the etching period evaluated and, second, independent control of lateral and vertical etching is not possible in conventional wet etching.

To highlight the advantage of the I-MacEtch mechanism and to explore the scalability of this method for the formation of nanostructures beyond practical lithography resolution and dry etch limitations, arrays of Au strips of ∼500 nm width and oriented 45° to the {110} planes are patterned by EBL. Under etching conditions with $\gamma$ = 24.5 at room temperature, ≤20 nm wide and ∼700 nm tall nanofins, as shown in Figure 8, are
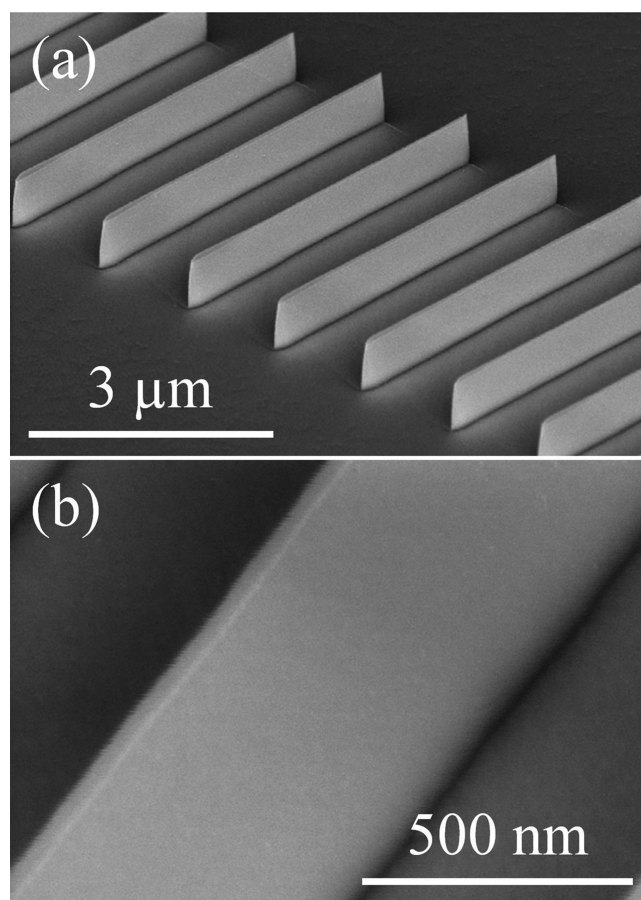


**Figure 8.** The 45° tilted-view SEM images of (a) an array of 20 nm wide InP nanofin structures fabricated by Au-catalyzed I-MacEtch in a $\gamma$ = 24.5 solution for 24 min. (b) zoomed-in view of one of the nanofins after Au etching and residual surface oxide etching.

produced after 24 min of etching. To the best of our knowledge, this is the first demonstration of InP nanofin arrays with ≤20 nm width scalability and high ARs, as well as smooth sidewalls, at room temperature by any etching technique. Even smaller dimensions can be achieved if the etching time is precisely controlled. The spacing between the nanofins is

limited by the lateral dimension of the metal pattern, which is the main limitation of this method.

In conclusion, we have demonstrated the formation of InP nanostructures with <20 nm and >35 AR scalability at room temperature by the I-MacEtch method. I-MacEtch is a unique and facile method to produce InP nanostructures, including linear, circular, and discrete features depending on the metal pattern, orientation, etchant composition, and etching time. On the basis of extensive TEM and XPS characterization, we believe that the inverse nature of this selective etching process is rooted in the formation of a thick oxide layer at the Au/InP interface that cannot be dissolved in the I-MacEtch solution. Remarkably, the sidewalls of the resultant nanostructures are not only nearly atomically smooth and free of porosity, but also are unaffected by the metal pattern edge roughness. I-MacEtch represents a highly economical and superior technique pertinent to the processing of various InP-based devices, including nanoscale field-effect transistors, solar cells, light emitters, and sensors.

## ■ ASSOCIATED CONTENT

### Ⓢ Supporting Information

Practical drawback of using Pt as a metal catalyst, influence of Au catalyst geometry as a function of etching depth, relevance of metal layer separation on surface morphology, photoluminescence experiment of InP nanopillars, SEM inspection of post-I-MacEtch XPS samples, curve-fitted photoelectron spectra and supplementary XPS analysis, residual oxide layer formed at Au/InP interface, comparison of hole injection barriers between Si and InP, and chemistry of I-MacEtch of InP in a mixture of $H_2O_2$ and $H_2SO_4$. This material is available free of charge via the Internet at http://pubs.acs.org.

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### Author Contributions

§S.H.K. and P.K.M. made equal contributions.

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

### Notes

The authors declare no competing financial interest.

## ■ ACKNOWLEDGMENTS

## ■ REFERENCES

(1) Li, X.; Bohn, P. W. *Appl. Phys. Lett.* **2000**, *77*, 2572.
(2) Huang, Z.; Geyer, N.; Werner, P.; de Boor, J.; Gösele, U. *Adv. Mater.* **2011**, *23*, 285−308.
(3) Li, X. *Curr. Opin. Solid State Mater. Sci.* **2012**, *16*, 71−81.
(4) Chun, I. S.; Chow, E. K.; Li, X. *Appl. Phys. Lett.* **2008**, *92*, 191113.
(5) Rykaczewski, K.; Hildreth, O. J.; Kulkarni, D.; Henry, M. R.; Kim, S.-K.; Wong, C. P.; Tsukruk, V. V.; Fedorov, A. G. *ACS Appl. Mater. Interfaces* **2010**, *2*, 969−973.
(6) DeJarld, M.; Shin, J. C.; Chern, W.; Chanda, D.; Balasundaram, K.; Rogers, J. A.; Li, X. *Nano Lett.* **2011**, *11*, 5259−5263.
(7) Mohseni, P. K.; Kim, S. H.; Zhao, X.; Balasundaram, K.; Kim, J. D.; Pan, L.; Rogers, J. A.; Coleman, J. J.; Li, X. *J. Appl. Phys.* **2013**, *114*, 064909.
(8) Balasundaram, K.; Mohseni, P. K.; Shuai, Y.-C.; Zhao, D.; Zhou, W.; Li, X. *Appl. Phys. Lett.* **2013**, *103*, 214103.
(9) Pinto, R.; Babu, R. S.; Bhattacharya, P. K. *Appl. Phys. Lett.* **1986**, *48*, 1427.
(10) Joshi, A. B.; Mann, E.; Chung, L.; Cho, T. H.; Min, B. W.; Kwong, D. L. *IEEE Trans. Semicond. Manuf.* **1998**, *11*, 495−500.
(11) Hu, H.; Mohseni, P. K.; Pan, L.; Li, X.; Somnath, S.; Felts, J. R.; Shannon, M. A.; King, W. P. *J. Vac. Sci. Technol., B* **2013**, *31*, 06FJ01.
(12) Wu, B.; Kumar, A.; Pamarthy, S. *J. Appl. Phys.* **2010**, *108*, 051101.
(13) Pecora, E. F.; Lawrence, N.; Gregg, P.; Trevino, J.; Artoni, P.; Irrera, A.; Priolo, F.; Dal Negro, L. *Nanoscale* **2012**, *4*, 2863−2866.
(14) Chern, W.; Hsu, K.; Chun, I. S.; de Azeredo, B. P.; Ahmed, N.; Kim, K.-H.; Zuo, J.; Fang, N.; Ferreira, P.; Li, X. *Nano Lett.* **2010**, *10*, 1582−1588.
(15) Irrera, A.; Artoni, P.; Iacona, F.; Pecora, E. F.; Franzò, G.; Galli, M.; Fazio, B.; Boninelli, S.; Priolo, F. *Nanotechnology* **2012**, *23*, 075204.
(16) Egatz-Gomez, A.; Majithia, R.; Levert, C.; Meissner, K. E. *RSC Adv.* **2012**, *2*, 11472.
(17) Peng, K.; Xu, Y.; Wu, Y.; Yan, Y.; Lee, S.-T.; Zhu, J. *Small* **2005**, *1*, 1062−1067.
(18) Garnett, E. C.; Yang, P. *J. Am. Chem. Soc.* **2008**, *130*, 9224−9225.
(19) Shin, J. C.; Chanda, D.; Chern, W.; Yu, K. J.; Rogers, J. A.; Li, X. *IEEE J. Photovoltaics* **2012**, *2*, 129−133.
(20) Zhang, B.; Wang, H.; Lu, L.; Ai, K.; Zhang, G.; Cheng, X. *Adv. Funct. Mater.* **2008**, *18*, 2348−2355.
(21) McSweeney, W.; Lotty, O.; Holmes, J. D.; O'Dwyer, C. *ECS Trans.* **2011**, *35*, 25−34.
(22) Huang, Z.; Fang, H.; Zhu, J. *Adv. Mater.* **2007**, *19*, 744−748.
(23) Hildreth, O. J.; Lin, W.; Wong, C. P. *ACS Nano* **2009**, *3*, 4033−4042.
(24) Chang, S.-W.; Chuang, V. P.; Boles, S. T.; Ross, C. a.; Thompson, C. V. *Adv. Funct. Mater.* **2009**, *19*, 2495−2500.
(25) Lai, C. Q.; Cheng, H.; Choi, W. K.; Thompson, C. V. *J. Phys. Chem. C* **2013**, *117*, 20802−20809.
(26) Oh, J.; Yuan, H.-C.; Branz, H. M. *Nat. Nanotechnol.* **2012**, *7*, 743−748.
(27) Huang, J.; Chiam, S. Y.; Tan, H. H.; Wang, S.; Chim, W. K. *Chem. Mater.* **2010**, *22*, 4111−4116.
(28) Lai, C.-C.; Lee, Y.-J.; Yeh, P.-H.; Lee, S.-W. *Nanoscale Res. Lett.* **2012**, *7*, 140.
(29) Geng, X.; Duan, B. K.; Grismer, D. A.; Zhao, L.; Bohn, P. W. *Electrochem. Commun.* **2012**, *19*, 39−42.
(30) Geng, X.; Duan, B. K.; Grismer, D. A.; Zhao, L.; Bohn, P. W. *Semicond. Sci. Technol.* **2013**, *28*, 065001.
(31) Lai, R.; Mei, X. B.; Deal, W. R.; Yoshida, W.; Kim, Y. M.; Liu, P. H.; Lee, J.; Uyeda, J.; Radisic, V.; Lange, M.; Gaier, T.; Samoska, L.; Fung, A. *Int. Electron Devices Meet.* **2007**, *3*, 609−611.
(32) Deal, W.; Mei, X. B.; Leong, K. M. K. H.; Radisic, V.; Sarkozy, S.; Lai, R. *IEEE Trans. Terahertz Sci. Technol.* **2011**, *1*, 25−32.
(33) Novotny, C. J.; Yu, E. T.; Yu, P. K. L. *Nano Lett.* **2008**, *8*, 775−779.
(34) Wallentin, J.; Anttu, N.; Asoli, D.; Huffman, M.; Aberg, I.; Magnusson, M. H.; Siefer, G.; Fuss-Kailuweit, P.; Dimroth, F.; Witzigmann, B.; Xu, H. Q.; Samuelson, L.; Deppert, K.; Borgström, M. T. *Science* **2013**, *339*, 1057−1060.
(35) Pearton, S. J.; Chakrabarti, U. K.; Baiocchi, F. A. *Appl. Phys. Lett.* **1989**, *55*, 1633.

(36) Hayes, T. R.; Dreisbach, M. A.; Thomas, P. M.; Dautremont-Smith, W. C.; Heimbrook, L. A. *J. Vac. Sci. Technol., B* **1989**, *7*, 1130.

(37) Monaico, E.; Tiginyanu, I.; Volciuc, O.; Mehrtens, T.; Rosenauer, A.; Gutowski, J.; Nielsch, K. *Electrochem. Commun.* **2014**, *47*, 29−32.

(38) Asoh, H.; Yokoyama, T.; Ono, S. *Jpn. J. Appl. Phys.* **2010**, *49*, 046505.

(39) Eliá, P.; Kosti, I.; Oltýs, J.; Hasenöhrl, S. *J. Micromech. Microeng.* **2004**, *14*, 1205−1214.

(40) Geng, X.; Duan, B. K.; Grismer, D. a; Zhao, L.; Bohn, P. W. *Semicond. Sci. Technol.* **2013**, *28*, 065001.

(41) Michaelson, H. B. *J. Appl. Phys.* **1977**, *48*, 4729.

(42) Williams, K. R.; Gupta, K.; Wasilik, M. *J. Microelectromech. Syst.* **2003**, *12*, 761−778.

(43) Zemek, J. *Thin Solid Films* **1993**, *224*, 141−147.

(44) Liu, H. C.; Tsai, S. H.; Hsu, J. W.; Shih, H. C. *J. Electrochem. Soc.* **1999**, *146*, 3510−3515.

(45) Faur, M.; Faur, M.; Jayne, D. T.; Goradia, M.; Goradia, C. *Surf. Interface Anal.* **1990**, *15*, 641−650.

(46) Kang, Y. S.; Kim, C. Y.; Cho, M.-H.; An, C.-H.; Kim, H.; Seo, J. H.; Kim, C. S.; Lee, T. G.; Ko, D.-H. *Electrochem. Solid-State Lett.* **2012**, *15*, G9−G11.

(47) Hollinger, G.; Bergignat, E.; Joseph, J.; Robach, Y. *J. Vac. Sci. Technol., A* **1985**, *3*, 2082.

(48) Shibata, N.; Ikoma, H. *Jpn. J. Appl. Phys.* **1992**, *31*, 3976.